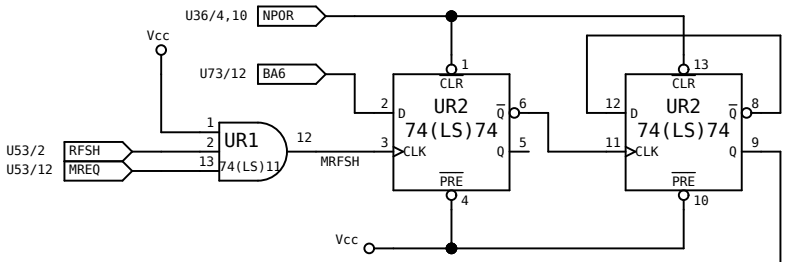
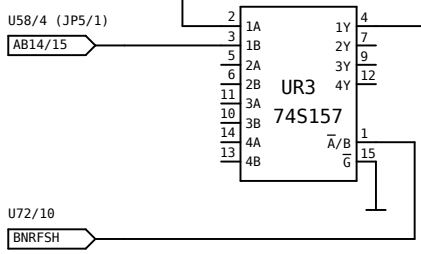
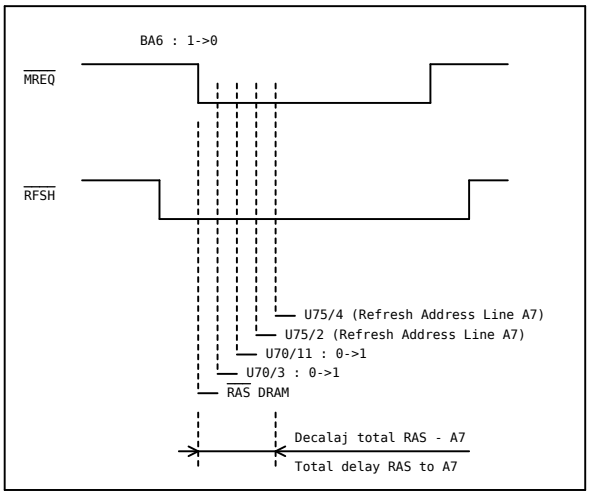


NOTA:
Acest circuit poate fi folosit cu placa de baza rev.3.16a, care insa nu are prevazute locuri de instalare pentru aceste componente (asamblare "in aer").

NOTE:
This circuit can be used with the mainboard rev.3.16a, but rev.3.16a does not have installation places for these components ("loose" assembly).





NOTE:

Due to the physical constraints related to the construction of the printed circuit board, the CPU address lines are not connected to the address inputs of the memories in the same order, but they are shuffled.
Thus, the correspondence between CPU address lines and the system memory address inputs (during refresh) is the following:

CPU Address	Memory Address
BA0	A0
BA1	A6
BA2	A1
BA3	A2
BA4	A3
BA5	A4
BA6	A5
AB14	A7

NOTA:

Datorita constringerilor fizice de realizare ale cablajului imprimat, liniile de adresa de la procesor nu sint legate in ordinea normala la intrarile de adrese ale memoriilor, ci amestecat.
Astfel, corespondenta intre linii de adresa procesor si linii adresa memorii sistem (pe durata refresh-ului) este:

Adrese CPU	Adrese memorii
BA0	A0
BA1	A6
BA2	A1
BA3	A2
BA4	A3
BA5	A4
BA6	A5
AB14	A7

Operation:

The diagram above shows the CPU refresh cycle corresponding to the changing of refresh address from 127 (7Fh, 1111111) to 0 (0000000) i.e. the change of refresh address bit 6 from 1 to 0. This change is detected by the circuit presented which "builds" the bit 7 of the refresh address by dividing the frequency of CPU refresh address bit A6 by 2.

In order to sample the CPU refresh address line BA6 correctly, a logical AND between signals MREQ and RFSH is used (signals already existing on the mainboard, generated by inverting $\overline{\text{MREQ}}$ and $\overline{\text{RFSH}}$) since the CPU refresh address lines are only guaranteed stable during $\overline{\text{MREQ}}$ activation (and $\overline{\text{RFSH}}$ of course).

The diagram above shows the consecutive delays through the 2 flip-flops and the multiplexer, as well as the delay of signal MREQ x RFSH from the falling edge of $\overline{\text{MREQ}}$, delay due to the inverters which generate signals MREQ and RFSH and due to gate U59/12.

Considering that the falling edge of $\overline{\text{MREQ}}$ is used as a RAS signal to the memory, all these delays cumulated add up to a total delay of the refresh addres bit A7 which is pretty significant.

Basically at the moment the refresh address changes from 127 to 0, bit A7 "produced" here for the 8-bit refresh address will not go from 0 to 1 soon enough to be part of the next logical refresh address (128).
Therefore the sequence of the refresh addresses generated will be:

128, 1, ... 127, 0, 129, ... 254, 255, 128, 1, ...

but this will still NOT affect the correct operation of the memory because the maximum refresh period will still be satisfied for all rows of the DRAM cell matrix.

Functionare:

Diagrama alaturata prezinta ciclul de refresh generat de procesor corespunzator schimbarii adresei de refresh de la 127 (7Fh, 1111111) la 0 (0000000) adica schimbarii bitului 6 de adresa refresh din 1 in 0. Aceasta schimbare este detectata de circuitul prezentat care "confectioneaza" bitul 7 de adresa refresh prin divizare cu 2 a frecventei liniei A6 de adresa pentru refresh de la procesor.

Pentru a esantiona corect linia de adresa BA6 de la procesor folosita pentru refresh se foloseste un SI logic intre MREQ si RFSH (semnale deja existente pe placa de baza, obtinute prin inversarea $\overline{\text{MREQ}}$ si $\overline{\text{RFSH}}$) intrucit liniile de adresa sint garantate stabile doar pe perioada activarii $\overline{\text{MREQ}}$.

In diagrama alaturata sint reprezentate intirzierile succesive prin cei doi bistabili si prin multiplexor, precum si intirzierea semnalului MREQ x RFSH fata de frontul negativ al $\overline{\text{MREQ}}$, intirziere datorata inversoarelor care genereaza MREQ si RFSH precum si portii U59/12.

Avind in vedere ca frontul negativ al $\overline{\text{MREQ}}$ este folosit ca semnal de RAS pentru memorie, toate aceste intirzieri cumulate provoaca o intirziere totala destul de semnificativa a bitului A7 de adresa pentru refresh.

Practic la momentul schimbarii adresei de refresh din 127 in 0, bitul A7 "confectionat" aici pentru adresa refresh pe 8 biti nu va trece din 0 in 1 suficient de rapid pentru a intra in componenta urmatoarei adrese de refresh (128).
Deci succesiunea adreselor de refresh generate va fi:

128, 1, ... 127, 0, 129, ... 254, 255, 128, 1, ...

dar asta nu va afecta buna functionare a memoriei intrucit tot se va respecta perioada maxima de refresh pentru toate liniile matricei de celule de memorie.

TITLE	µC CoBra - Refresh RAS-Only pe 8 biti CoBra µC - 8-bit RAS-Only Refresh		
FILE:	CoBra	REVISION:	3.16a (test, 64/80KB DRAM)
PAGE	1 OF 1	DRAWN BY:	ElectroNNix